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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,475	08/29/2001	Hideki Sawaguchi	ASAM.0019	4883
38327 75 REED SMITH L	590 02/15/200 LP	EXAMINER		
3110 FAIRVIEW	V PARK DRIVE, SUI	RODRIGUEZ, GLENDA P		
FALLS CHURCH, VA 22042			ART UNIT	PAPER NUMBER
			2627	
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SHORTENED STATUTORY	PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

		Application No.	Applicant(s)	
Office Action Summary		09/940,475	SAWAGUCHI ET AL.	
		Examiner	Art Unit	
		Glenda P. Rodriguez	2627	
Period fo	The MAILING DATE of this communication apports.	pears on the cover sheet with the c	correspondence address	
A SH WHIC - Exter after - If NC - Failu Any (ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DANSIONS of time may be available under the provisions of 37 CFR 1.1. SIX (6) MONTHS from the mailing date of this communication. Operiod for reply is specified above, the maximum statutory period or re to reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tin will apply and will expire SIX (6) MONTHS from , cause the application to become ABANDONE	N. nely filed the mailing date of this communication. ED (35 U.S.C. § 133).	
Status			·	
2a)⊠	Responsive to communication(s) filed on 30 N. This action is FINAL . 2b) This Since this application is in condition for allowar closed in accordance with the practice under Expression 1.	action is non-final.		
Dispositi	on of Claims			
5)⊠ 6)⊠ 7)⊠ 8)□ Applicati 9)□	Claim(s) 1-24, 27-46 is/are pending in the apple 4a) Of the above claim(s) is/are withdraw Claim(s) 27-42 is/are allowed. Claim(s) 1,6-12,17-26 and 43-46 is/are rejecte Claim(s) 2-5 and 13-15 is/are objected to. Claim(s) are subject to restriction and/or on Papers The specification is objected to by the Examine The drawing(s) filed on is/are; a) according to the province of the province o	wn from consideration. d. r election requirement.	Evaminar	
_	The drawing(s) filed on is/are: a) according a second and a second a second and a second a second and a second a second and a second a second and a second a second and a second a se	drawing(s) be held in abeyance. Section is required if the drawing(s) is ob-	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).	
Priority u	ınder 35 U.S.C. § 119			
12) [a)[Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority document: 2. Certified copies of the priority document: 3. Copies of the certified copies of the priority document: application from the International Bureau See the attached detailed Office action for a list	s have been received. s have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	ion No ed in this National Stage	
2) (Notic 3) (Inform	e of References Cited (PTO-892) se of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO/SB/08) or No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Do 5) Notice of Informal F 6) Other:	ate	

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DETAILED ACTION

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 1, 6-9, 12, 17-20 and 43-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziperovich (US Patent No. 5, 459, 679) in view of Mallary (US Patent No. 6, 359, 744).

Regarding Claim 1, Ziperovich teaches a magnetic recording/reproducing apparatus comprising a medium and a reproducing head constituted by a magneto resistive effect type head with a shield film (Elements 12 and 10),

Wherein a reproduced signal outputted from said reproducing head is processed through a partial response equalization circuit (Col. 5, L. 21-27, wherein Ziperovich teaches a PRML channel) having a frequency characteristic so that a low-frequency component of said reproduced signal including a direct current component is passed and suppressed through said partial response equalization circuit (See Col. 8, under DC Offset Control Loop, wherein Ziperovich teaches how the PRML channel cancels the Offset of the signal. It is obvious that because the DC offset is found at frequency value 0, when the DC offset is eliminated, the low frequencies are also diminished or eliminated when eliminating the DC offset.);

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And wherein said reproduced signal is supplied to a maximum-likelihood decoder so as to be data-reproduced (Col. 1, L. 50-65, wherein it describes that PRML channels contain ML of Maximum Likelihood detectors.).

However, Ziperovich does not explicitly teach that the medium is a dual layer perpendicular medium and it has a soft underlayer. Mallary teaches a perpendicular dual layer medium with a soft underlayer in Elements 30, 115 and 120. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Ziperovich's invention with the teaching of Mallary in order to increase data storage capacity as taught by Mallary in the Summary of the invention.

Claim 12 has limitations similar to those treated in the above rejection, and is met by the references as discussed above.

Regarding Claims 6 and 17, the combination of Ziperovich and Mallary teach all the limitations of Claims 1 and 12, respectively. The combination further teach wherein comprising a plurality of partial response equalization circuits having different direct current frequency component passing characteristics respectively or a plurality of partial response equalization circuits defined by different values of parameter a respectively, wherein a reproduced signal from said reproducing head is supplied to said plurality of partial response equalization circuits so as to be waveform-equalized in said partial response equalization circuits (Col. 6, L. 2-14 of Ziperovich).

Regarding Claims 7 and 18, the combination of Ziperovich and Mallary teach all the limitations of Claims 1 and 12, respectively. The combination further teach one of different direct current frequency component passing characteristics or one of different values of

parameter a is selected and set in said partial response equalization circuit, and wherein said reproduced signal from said reproducing head is supplied to said partial response equalization circuit so as to be waveform-equalized (Col. 6, L. 2-14 of Ziperovich).

Regarding Claims 8, 19, 43 and 45, the combination of Ziperovich and Mallary teach all the limitations of Claims 6, 17, 18 and 7, respectively. The combination further teach wherein at least one of said different direct current frequency component passing characteristics is a cut-off characteristic of a direct current frequency component, or at least one of different values of said parameter α satisfies a condition of $\alpha=1$ (Col. 12, L. 56-63 of Ziperovich).

Regarding Claims 9, 20, 44, 46, the combination of Ziperovich and Mallary teach all the limitations of Claims 8, 19, 43 and 45, respectively. The combination further teach wherein a signal for adjusting or controlling a circuit disposed in a pre-stage of said partial response equalization circuit is referred to from a circuit in a post-stage of said partial response equalization circuit having said cut-off characteristic of said DC frequency component, or from a circuit in a post-stage of said response equalization circuit having said parameter a satisfying α =1 (Col. 8, under "DC Offset Control Loop", wherein Ziperovich teaches the post stage equalization of the signal in order to eliminate the offset. See also Col. 12, L. 56-63 of Ziperovich).

3. Claims 10, 11, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ziperovich and Mallary as applied to claim 1 above, and further in view of Hull et al. (US Patent No. 6, 262, 857).

Regarding Claims 10 and 21, the combination of Ziperovich and Mallary teach all the limitations of Claims 1 and 12, respectively. However, the combination does not explicitly teach wherein an information data bit sequence to be recorded is converted into a data bit sequence so

that a maximum number m of consecutive recording transitions recorded at a shortest bit length interval on said recording medium is limited to a finite value; and then said converted data bit sequence is recorded on said recording medium. This limitation is taught by Hull et al., wherein its Gray code (which is a finite amount of data) is written in the shortest bit length as taught in Col. 35, L. 1-7. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of Hull et al. in order to detect its position in a disk as taught in Col. 34, L. 61-65.

Regarding Claims 11 and 22, the combination of Ziperovich, Mallary and Hull et al. teach all the limitations of Claims 10 and 21, respectively. The combination further teach wherein the transitions cannot be larger than 4 (Col. 34, L. 61-65. It is obvious that the Gray code can be adjusted to a finite amount of bits.).

4. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ziperovich and Mallary as applied to claim 12 above, and further in view of Kikuta (US Patent No. 6, 377, 416).

Regarding Claim 23, the combination of Ziperovich and Mallary teach all the limitations of Claim 12. However, the combination does not explicitly teach wherein a semiconductor integrated circuit. This is taught by Kikuta in Col. 1, L. 9-16. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of Kikuta in order to have faster reading/writing speeds as taught by Kikuta in the Background of the Invention.

Regarding Claim 24, the combination of Ziperovich, Mallary and Kikuta teach all the limitations of Claim 23. The combination further teach wherein a semiconductor is mounted thereon (See Col. 1, L. 9-16 of Kikuta).

Allowable Subject Matter

5. Claims 2-5, 13-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reasons for allowable subject matter were cited in the previous Office Action.

6. Claims 27-42 are allowed.

The reasons for allowance were cited in the previous Office Action.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

7. Applicant's arguments filed 11/30/06 have been fully considered but they are not persuasive. Applicant argues that contrary to Ziperovich which was the reference used by the Examiner, the present application is a "...structure that passes and suppresses the DC component. This distinction means the DC component is attenuated and appropriately controlled- not made zero as in Ziperovich". Examiner cannot concur with the Applicant due that according to Webster's Dictionary, the verb suppress under the definition number 5

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(Electronics, Radio, etc) means 'to eliminate or weaken'. Therefore, the cited reference Ziperovich according to the definition, is in fact suppressing the DC component. Therefore, the USC 103 under the combination of Ziperovich and Mallary stands.

8. Examiner acknowledges that Claims 25 and 26 have been canceled.

Conclusion

9. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (571) 272-7561. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea L. Wellington can be reached on (571) 272-4483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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gpr 02/07/07 ANDREA WELLINGTON
SUBERVISORY PATENT EXAMINER